The MROD

The MDT Precision Chambers ROD

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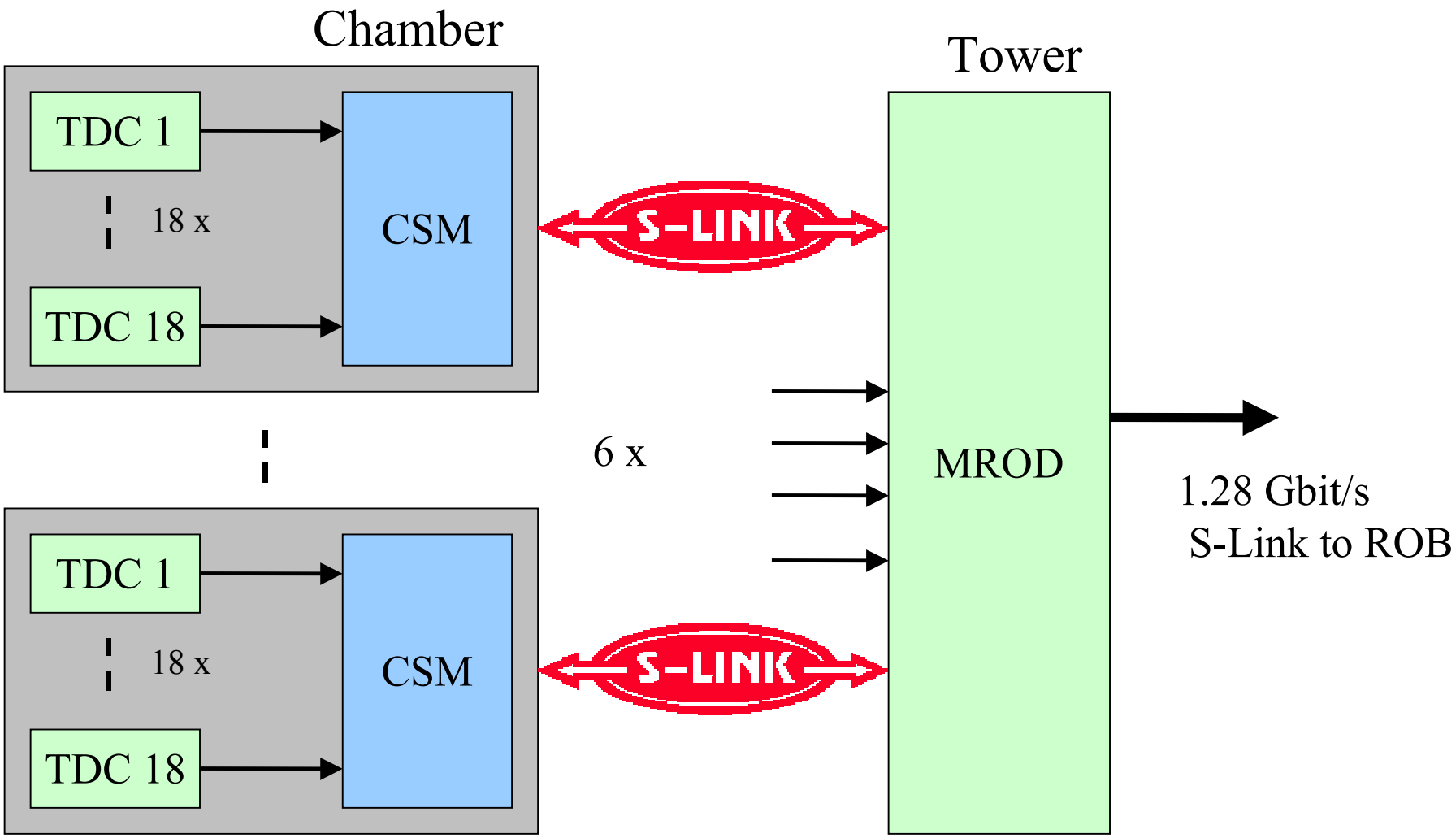
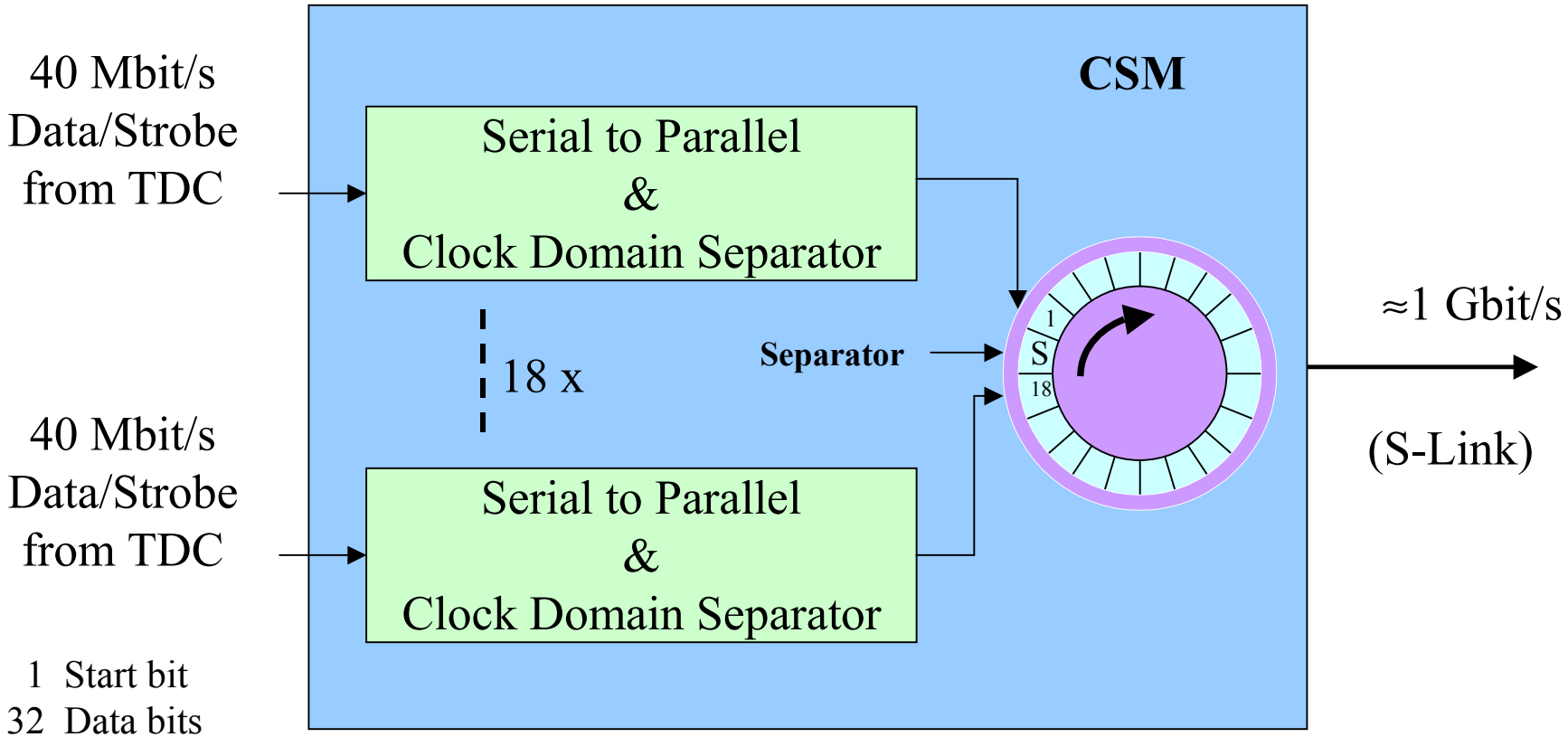
System Overview



TDC Functionality

- 24 channels, 0.78 ns bin size
- entirely data driven: records time stamp for each hit (leading and/or trailing edges)
- stores hits in internal derandomizing buffer
- upon receipt of a L1A, it ouputs the relevant hit data words on a serial output link (40 Mbit/s) with header and trailer words

CSM Functionality

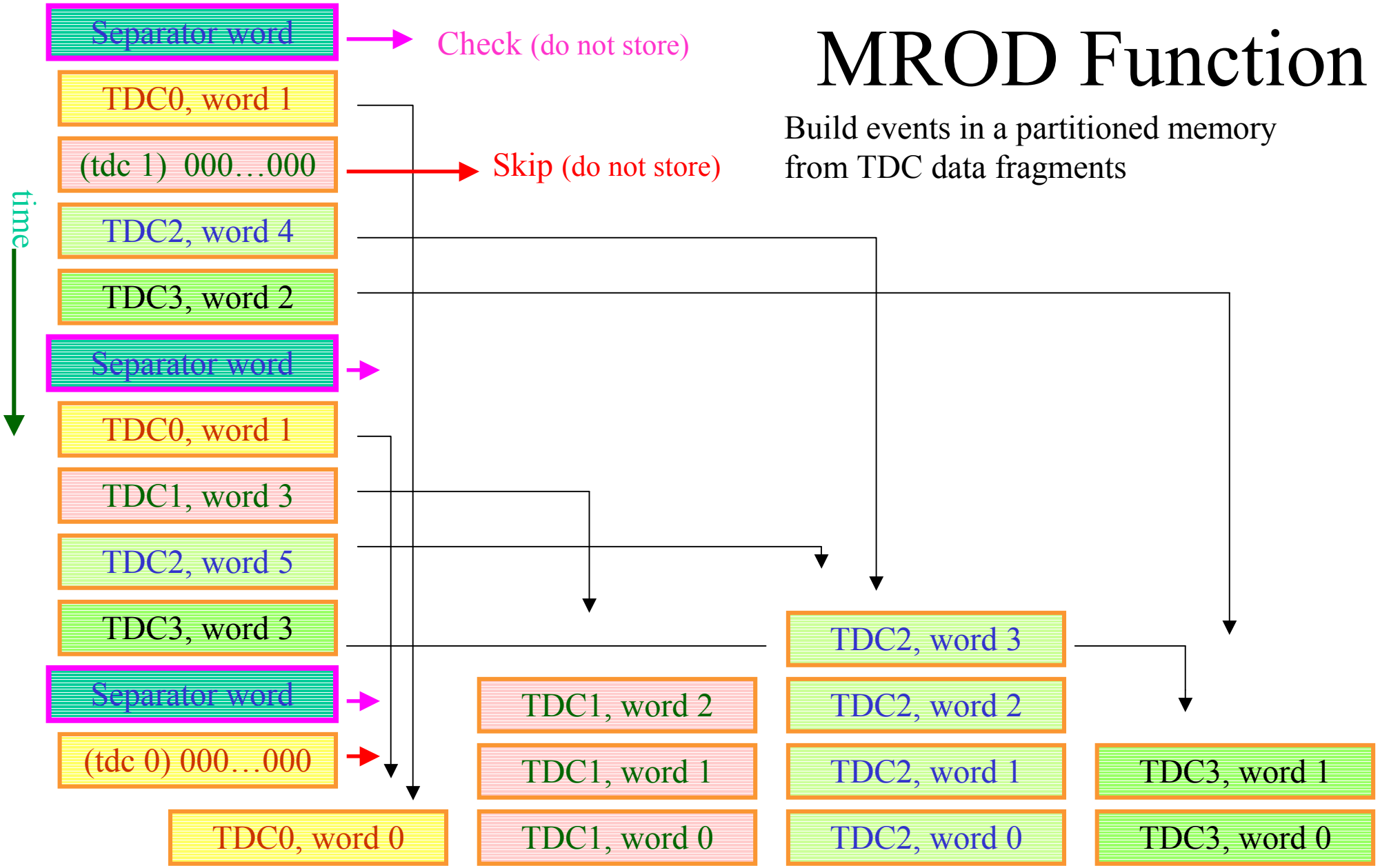


1 Start bit
32 Data bits
1 Parity bit
1 Stop bit
35 bits @ 25 ns = 875 ns

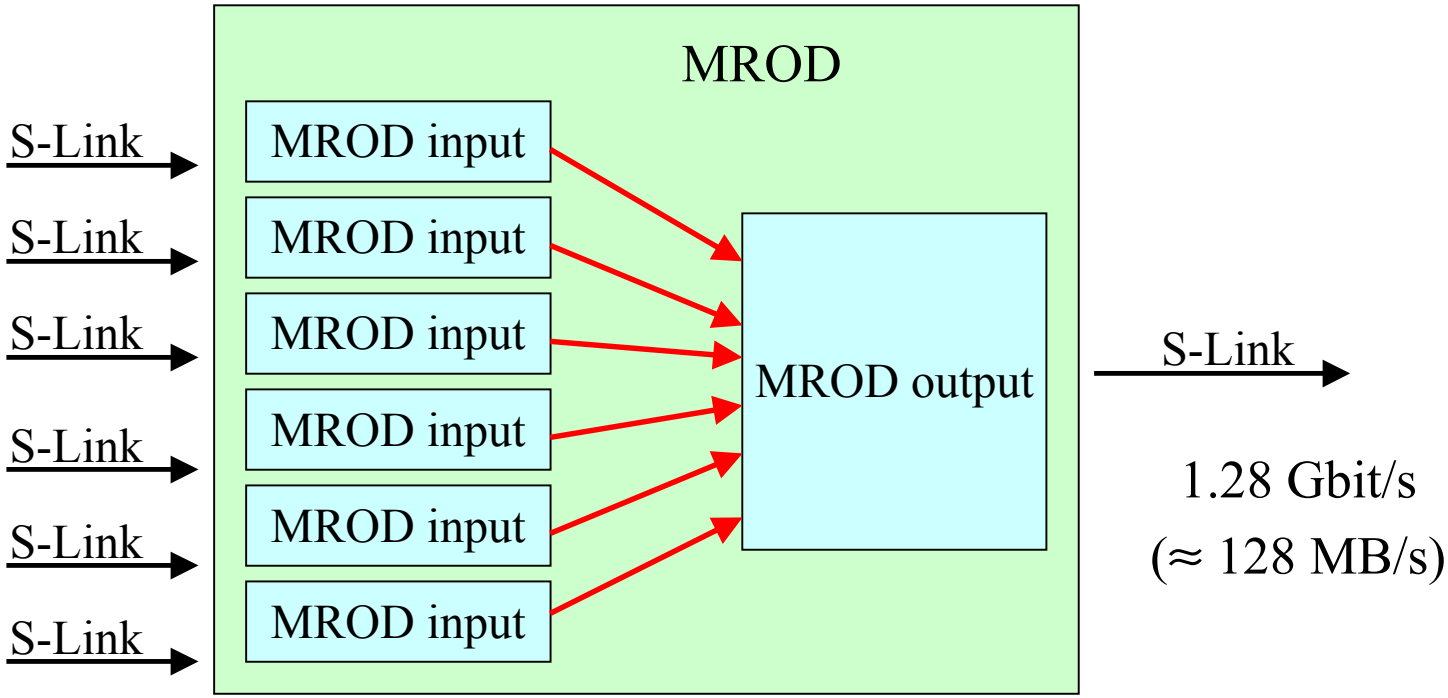
1 Separator word (S)
18 TDC data words
19 words in 875 ns → 87 MB/s

MROD Function

Build events in a partitioned memory
from TDC data fragments



MROD Throughput



Average 5 hits per TDC + header + trailer = 7 words/event
Per tower of 6 chambers max. 88 TDCs * 7 ≅ 600 words/event (= 2.4 kB/event)
Worst case est.: @ 100 kHz L1A rate → 240 MB/s per MROD
Calculation based on actual tower layout (J.Chapman): max. rate < 60 MB/s per MROD

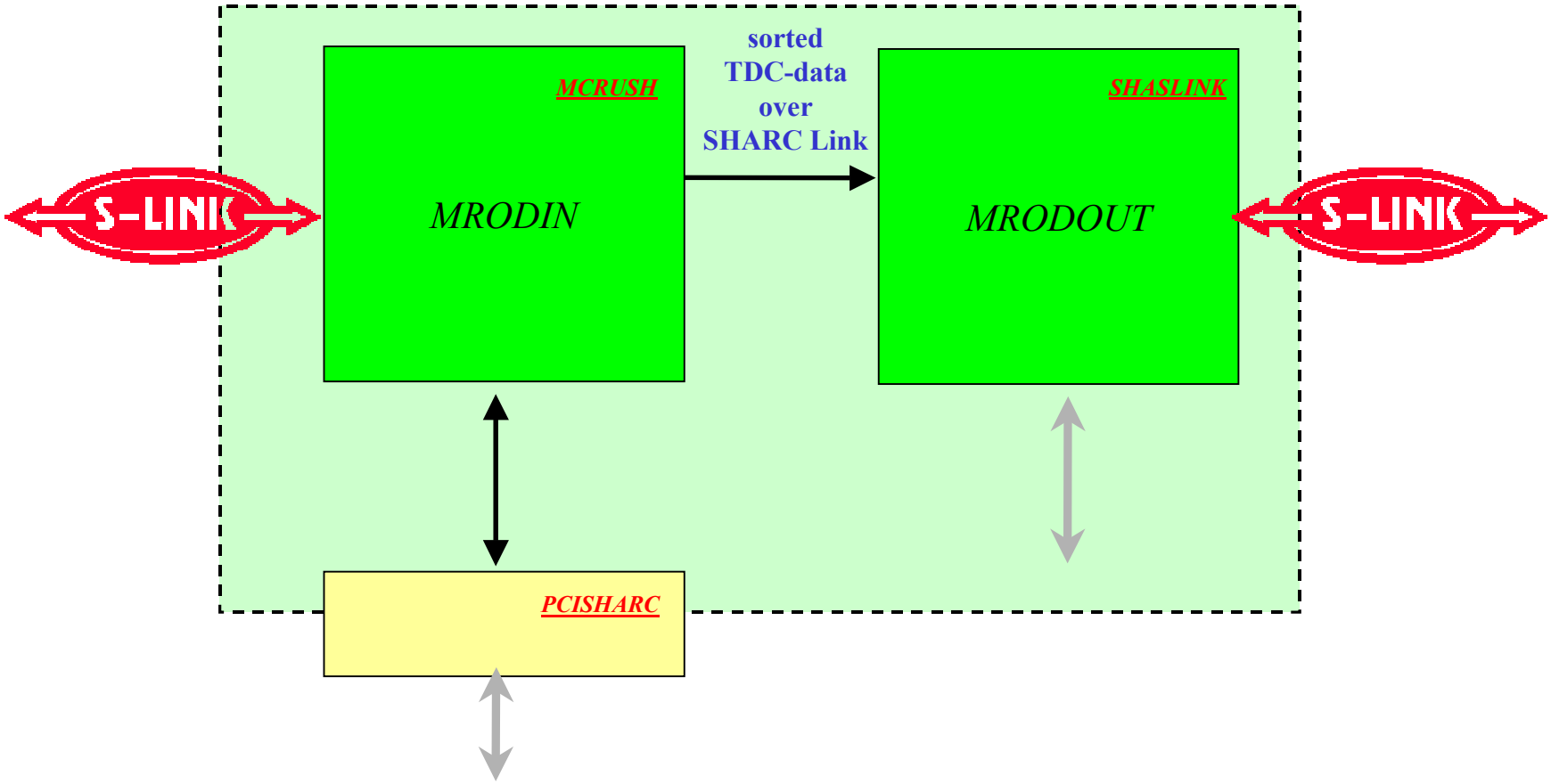
MROD Form Factor

- 9 U VME board (single slot), 6 inputs, 1 output
- Optionally 2 extra inputs with “extension” board
  to accommodate special towers (> 6 chambers)
- S-link interfaces on main board
- SHARC II (ADSP21160), 2.5 x faster than 21060

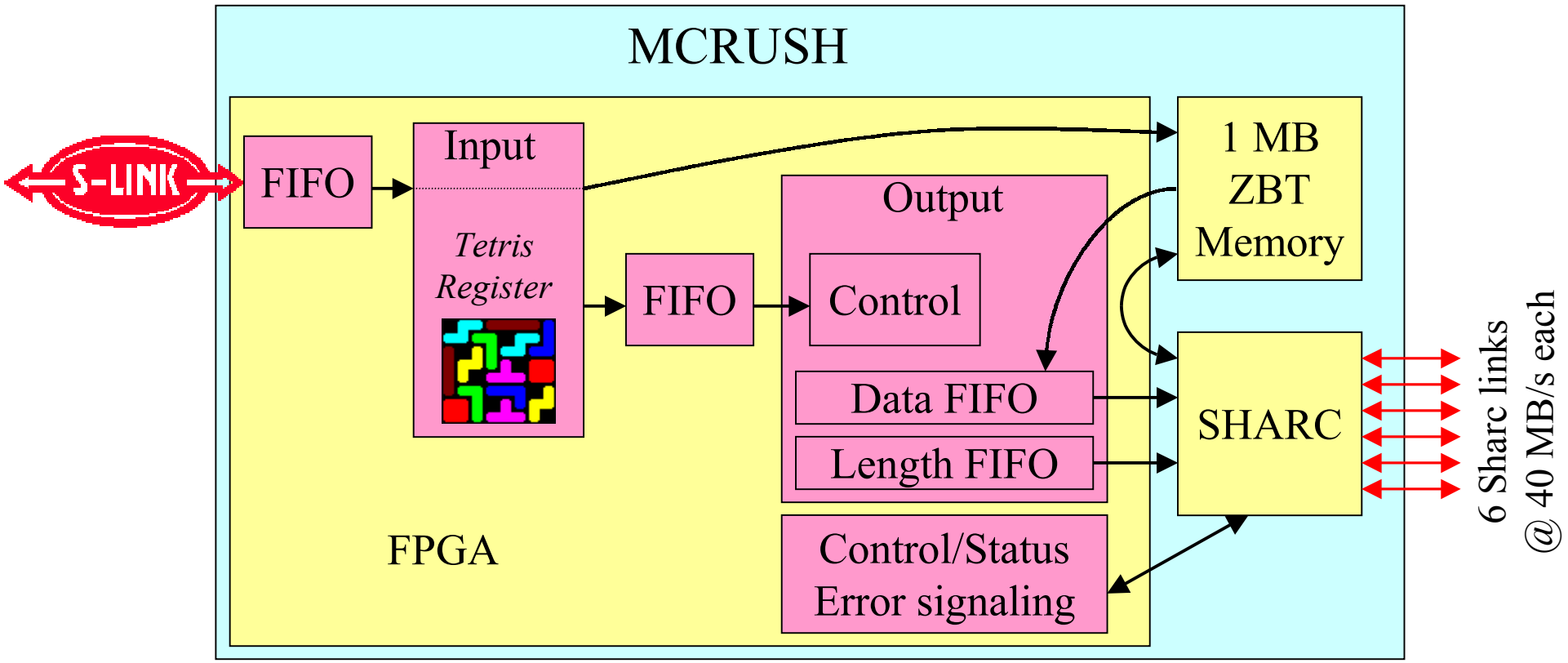
- 1 MROD Crate contains:
  12 MRODs (12 η Segments)
  Max. 4 MROD Extension Boards
  1 Standard (?) Crate Master with Ethernet Interface (DetDAQ)
  1 TTC-Rx Interface Module
  1 Busy Module ??
  1 DCS Interface Module ??

- @ 192 towers: 192/12 = 16 MROD Crates (1 per φ Sector)

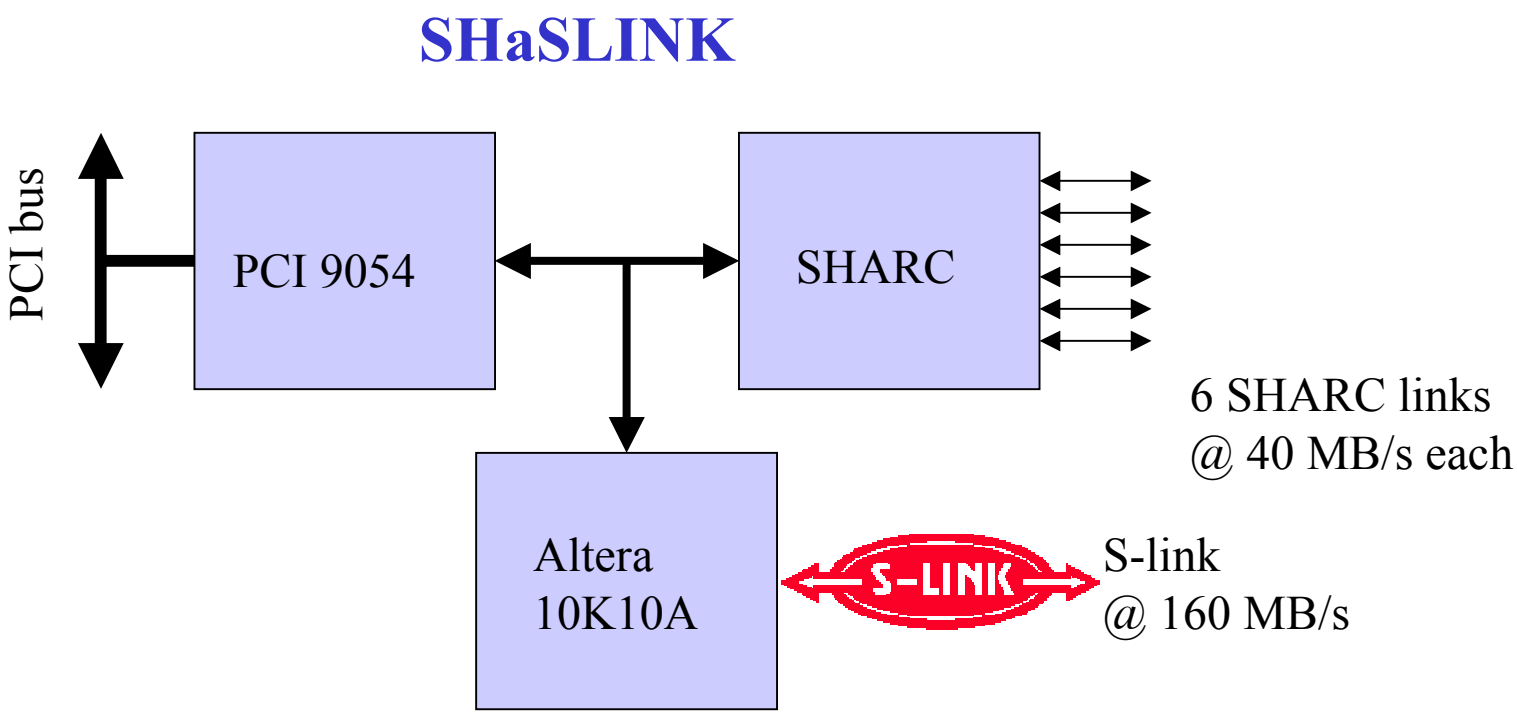
MROD-0 Prototype



MROD-0 Input Channel



MROD-0 Output Channel



ADSP-21060/ADSP-21062 (SHARC)

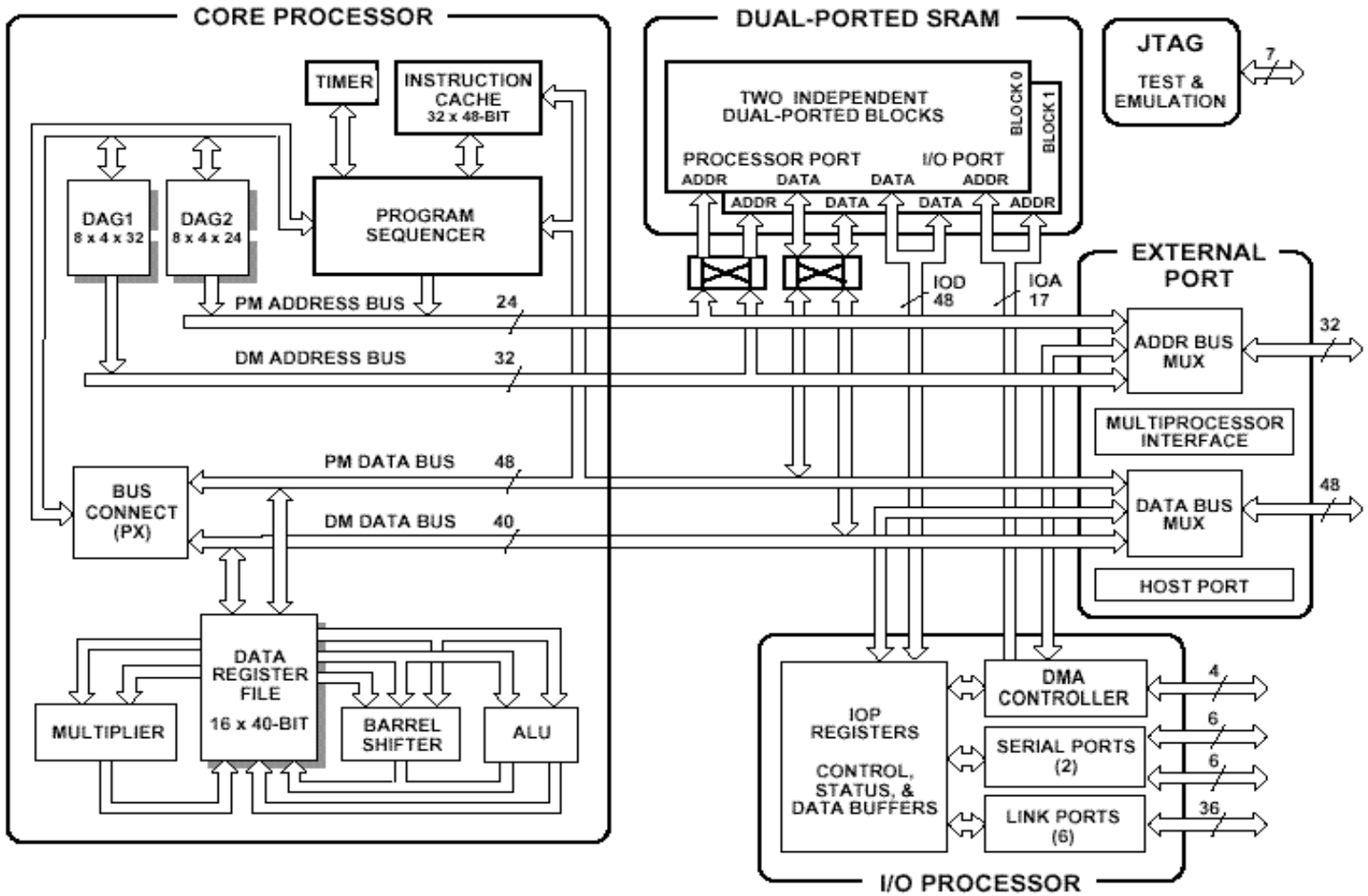
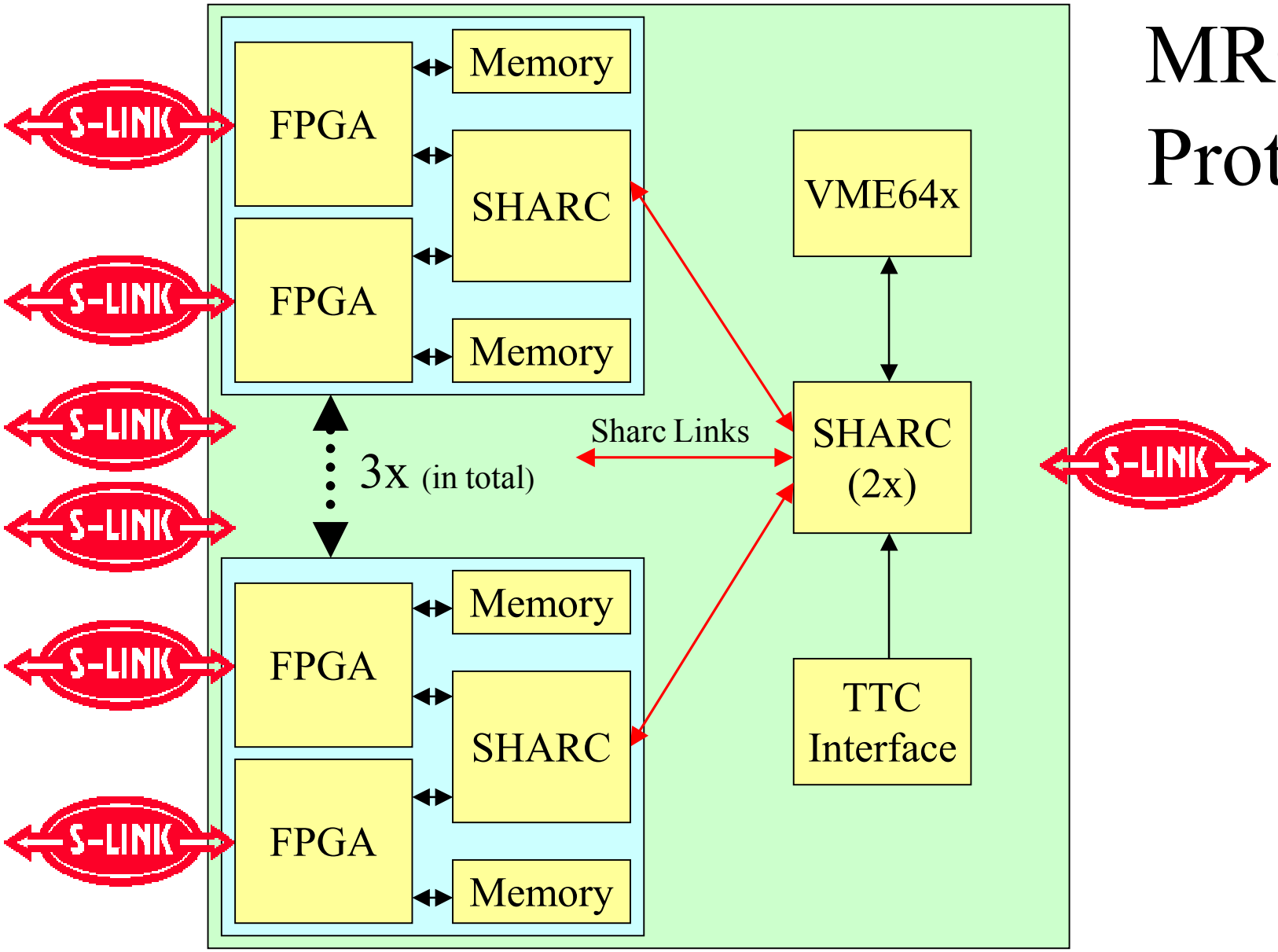


Figure 1. ADSP-21060/ADSP-21062 Block Diagram

MROD-1 Prototype



SHARC-II

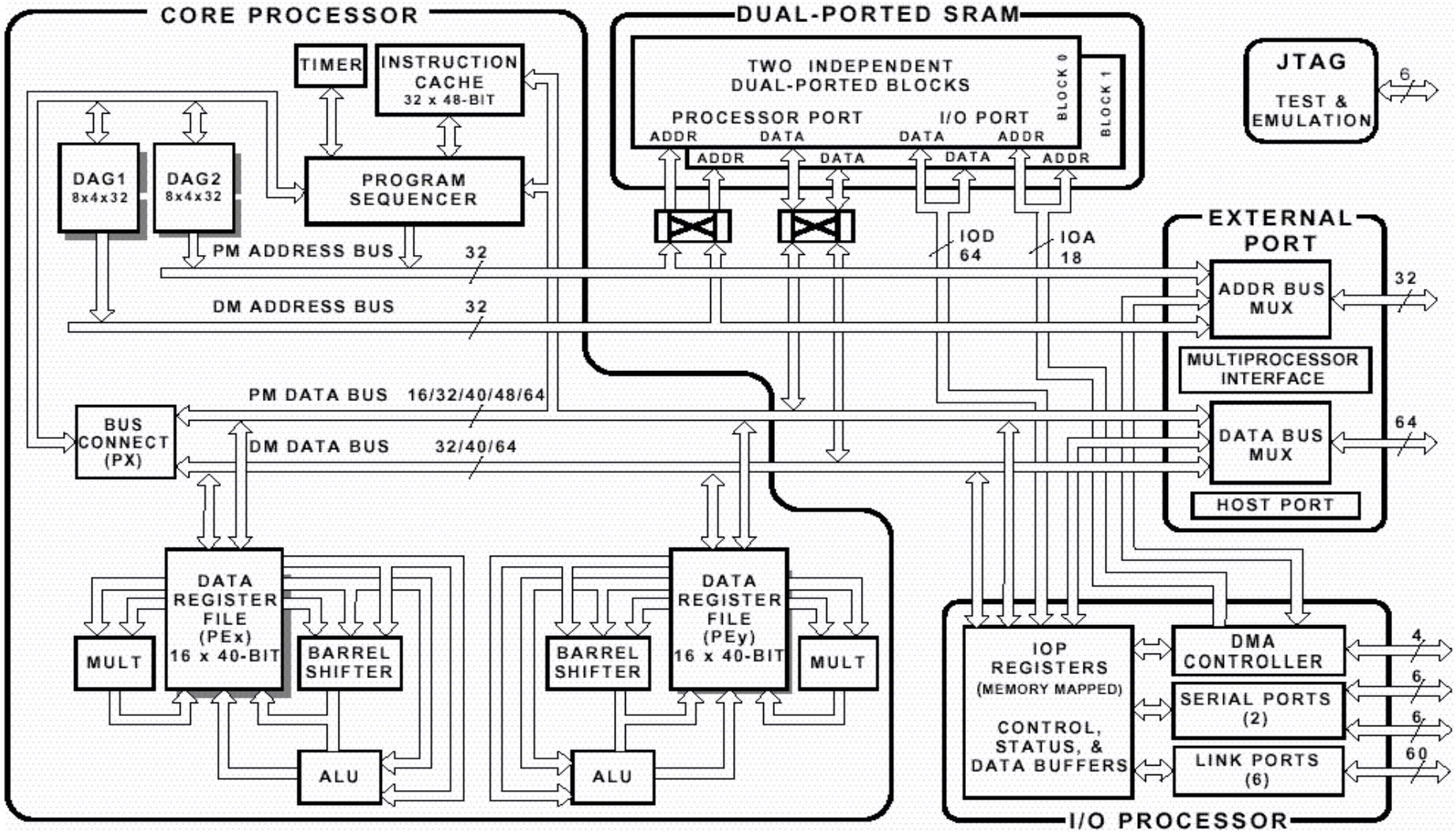


Figure 1 ADSP-21160 Functional Block Diagram

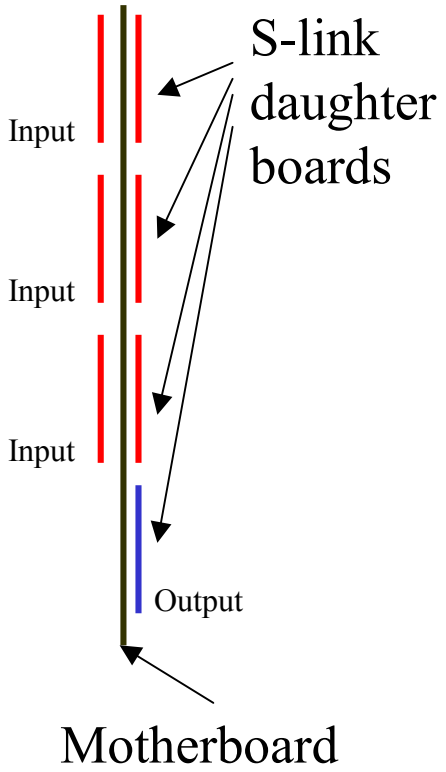
The ADSP-21060 and the ADSP-21160 SHARCs

- 40 MHz / 80 → 100 MHz CPU (SIMD mode)
- 512 KB / 512 KB internal memory
- **6 x** 40 / 80 → 100 MB/s links. Throughput of all links simultaneously is 160 / 480 → 600 (?) MB/s, without disturbing the CPU.
- No handshaking on links, but hardware XON-XOFF protocol,
- 10 / 14 DMA channels
- Support for bus arbitration: at max. 6 SHARCs can be connected to a common bus without glue logic. Each SHARC can access the internal memories of each other SHARC. The SHARCs also provide support for a so-called host interface, which can act as an additional master on the common bus.
- Fast interrupt servicing due to the presence of shadow registers
- Two 40 Mbit/s / 40 → 50 Mbit/s (at max.) synchronous serial ports
- Can be booted via link 4

MROD-1 Form Factor

- 9 U VME board, 6 inputs, 1 output
- S-link interfaces on daughter boards

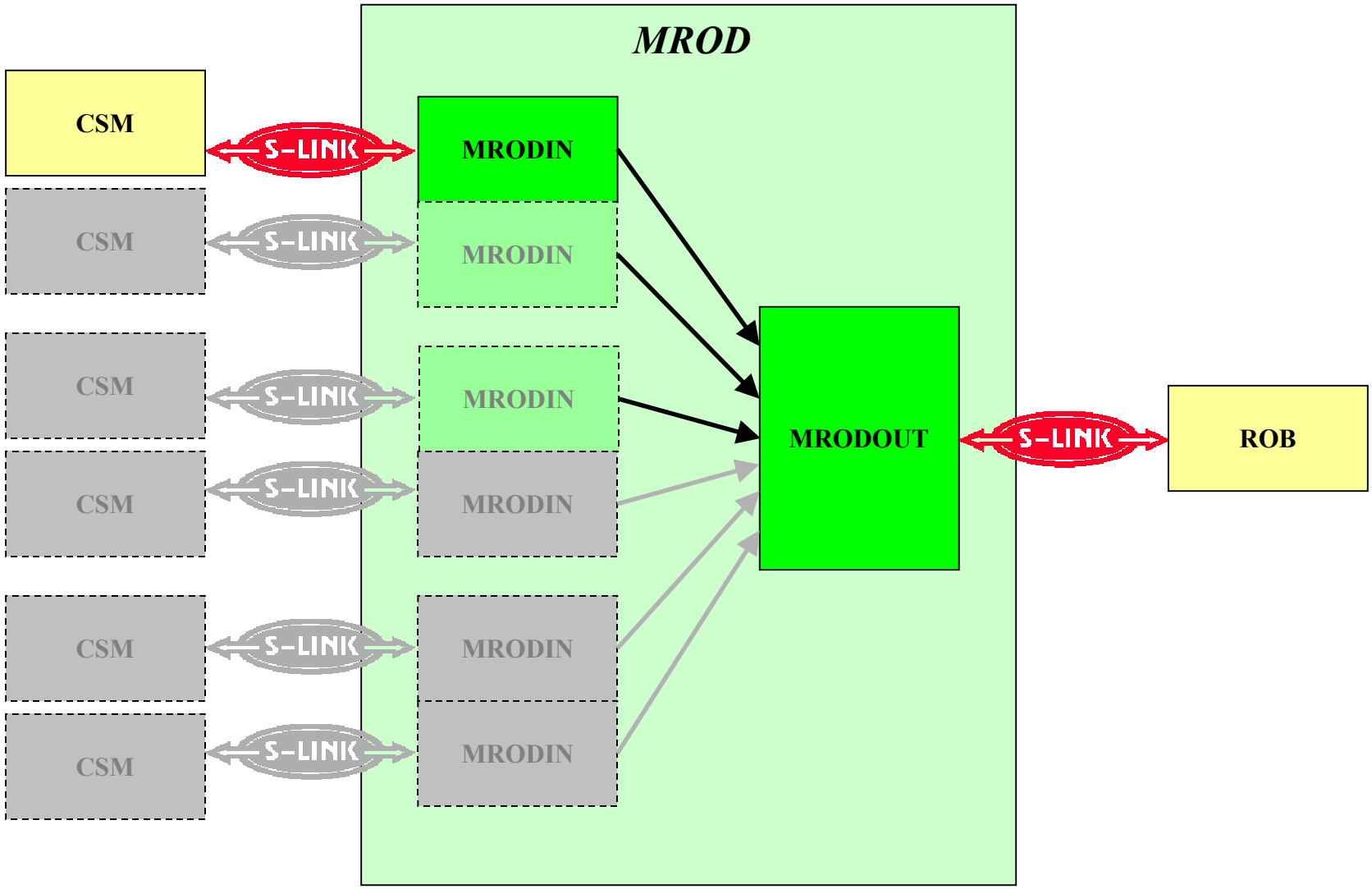
- SHARC II (ADSP21160), 2 x faster than 21060
  (3 for input, 2 for output processing)
- Altera APEX FPGAs, 200k gates
- TTC interface (over back plane)
- VME64x interface



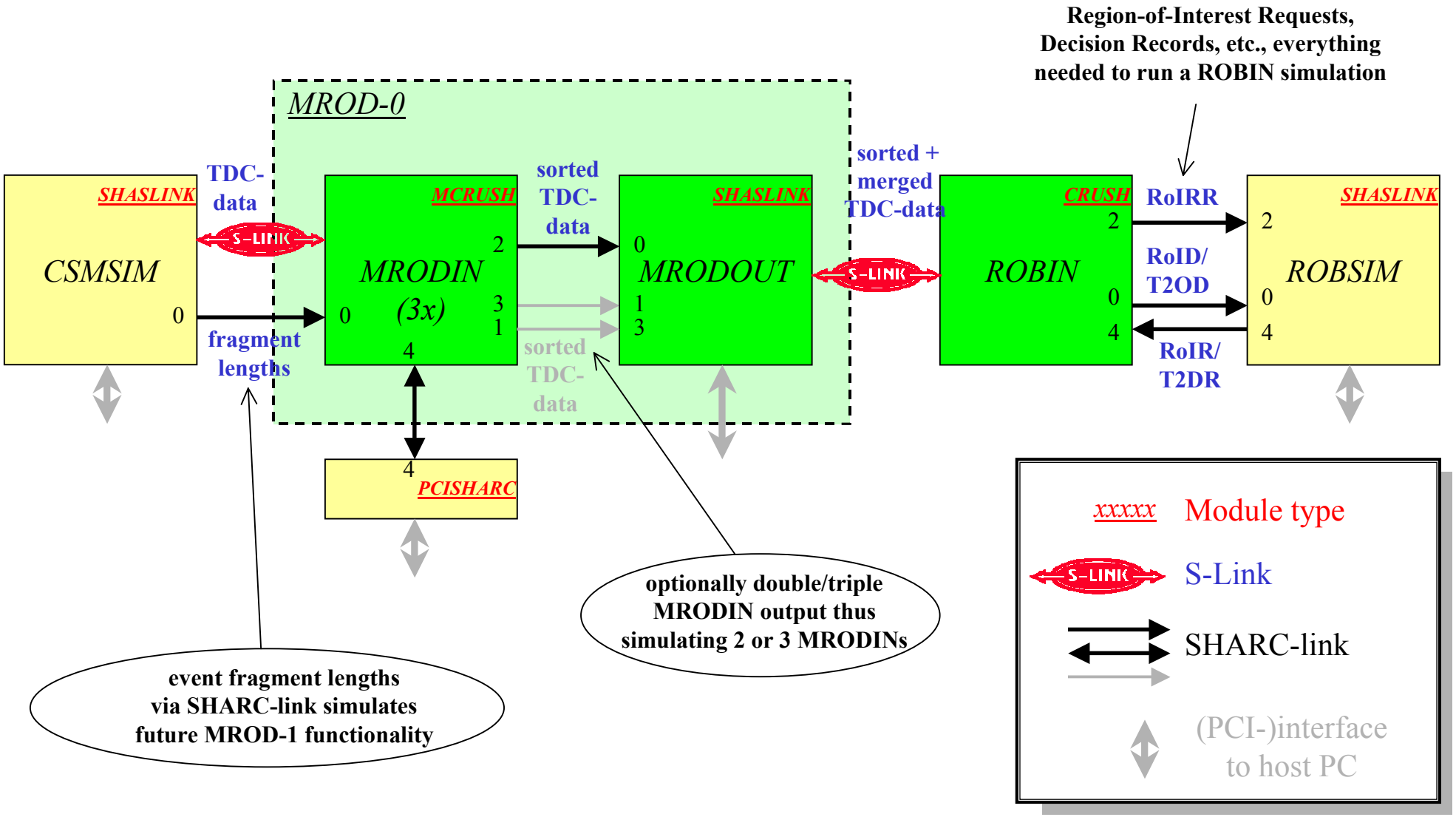
MROD-1 Status & Planning

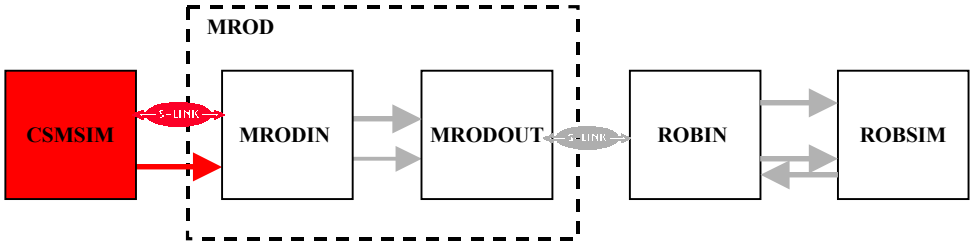
- VHDL design of FPGAs almost finished.
- Modules available by 1st April 2001.
- Extensive tests and performance measurements at NIKHEF.
- System integration tests with CSM.
- System integration tests with ROB and DAQ test set-up (possibly in test-beam).
- Read out of BOL test stand at NIKHEF.

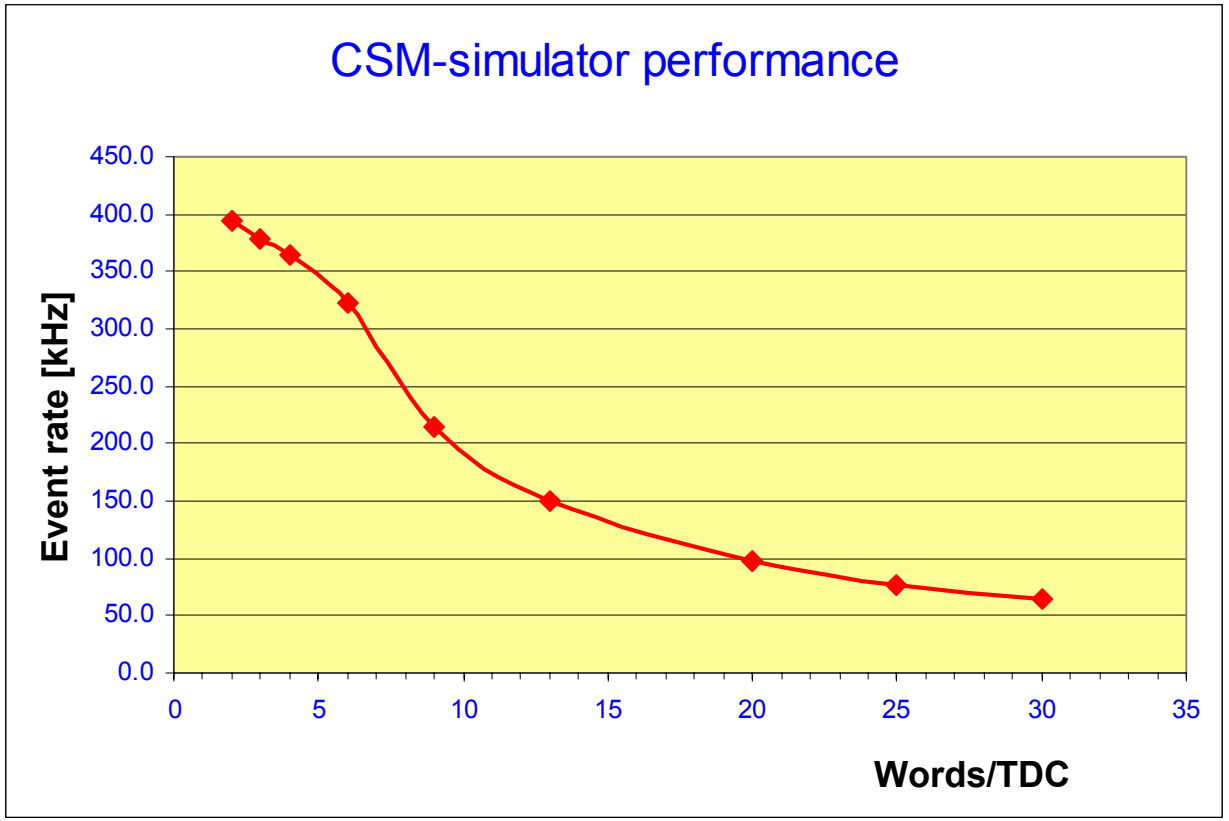
MROD Performance Study



MROD Emulation Hardware

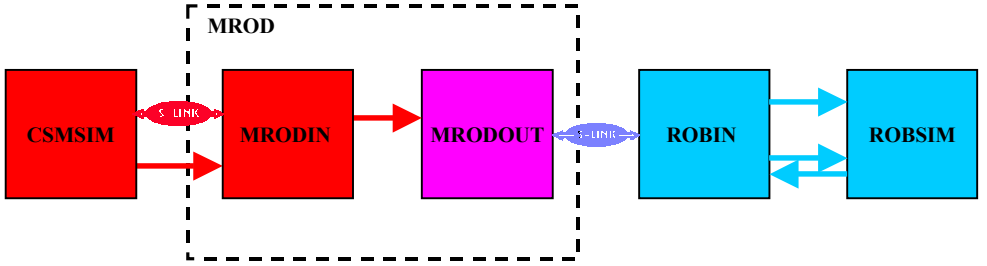


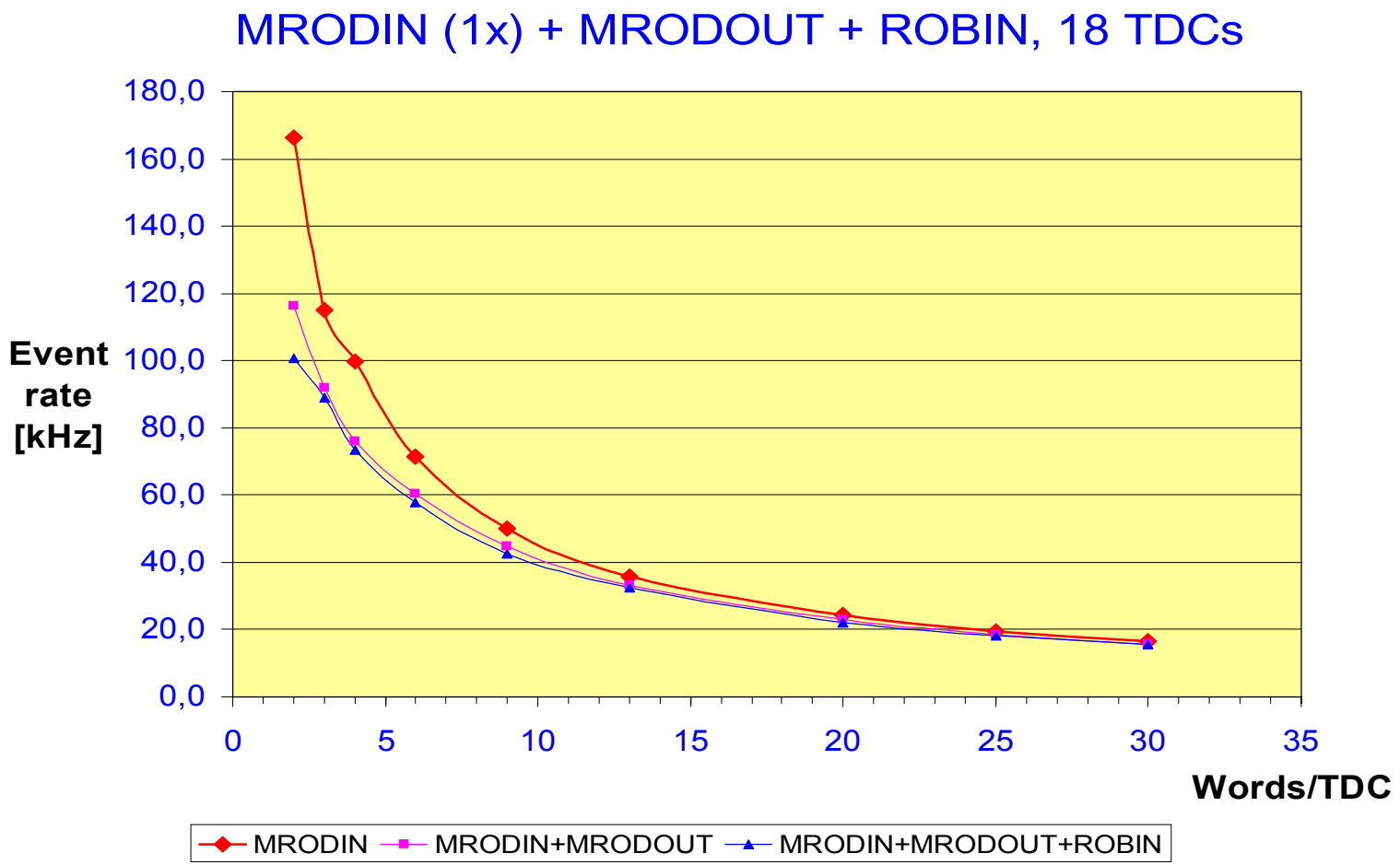

MROD
CSMSIM
S-LINK
MRODIN
MRODOUT
S-LINK
ROBIN
ROBSIM


CSM-simulator performance
Event rate [kHz]
450.0
400.0
350.0
300.0
250.0
200.0
150.0
100.0
50.0
0.0
0
5
10
15
20
25
30
35
Words/TDC

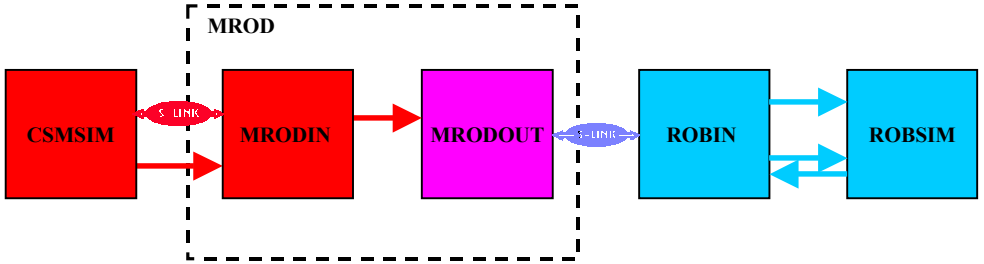
MROD

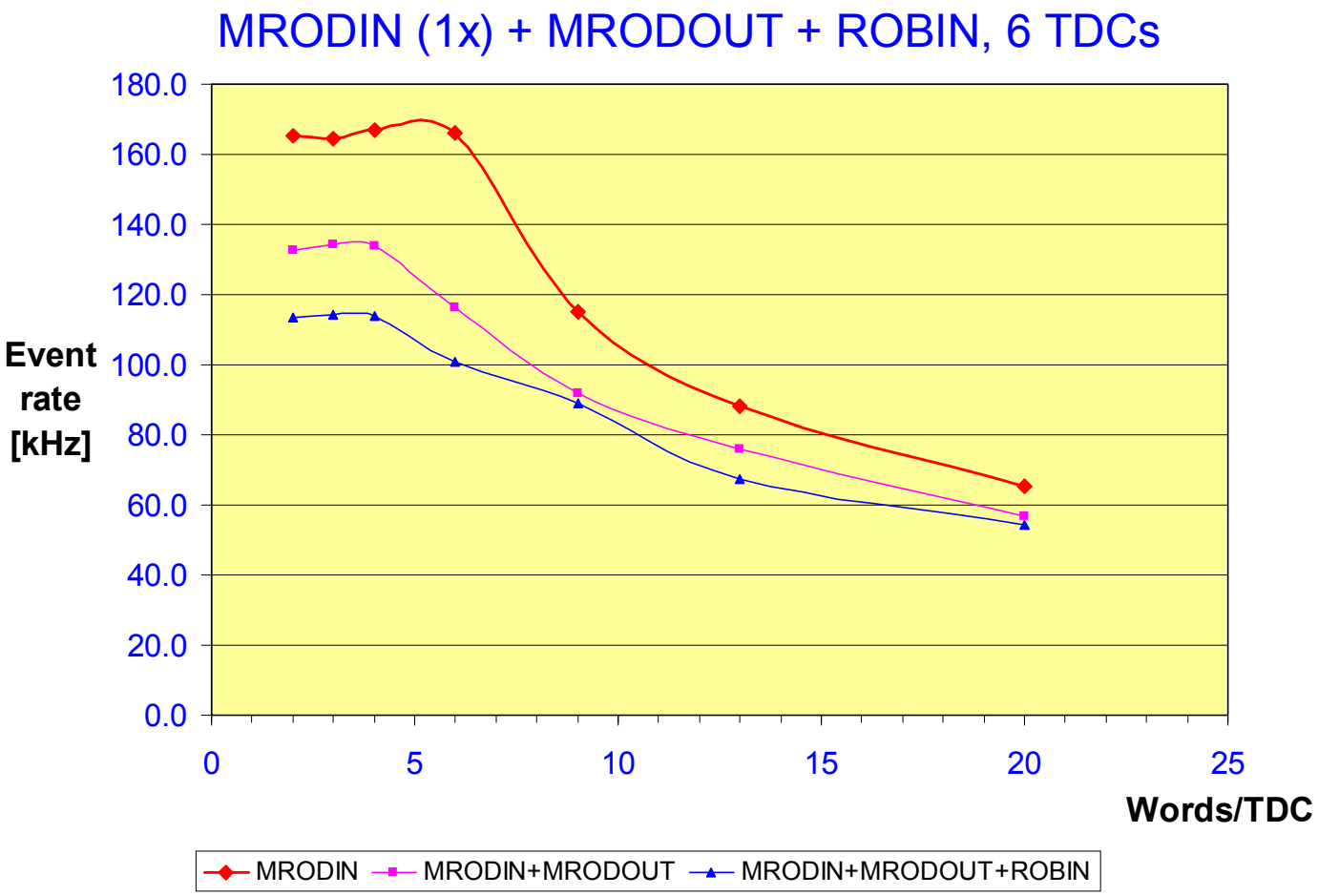
Performance Study Results





MROD
Performance Study Results





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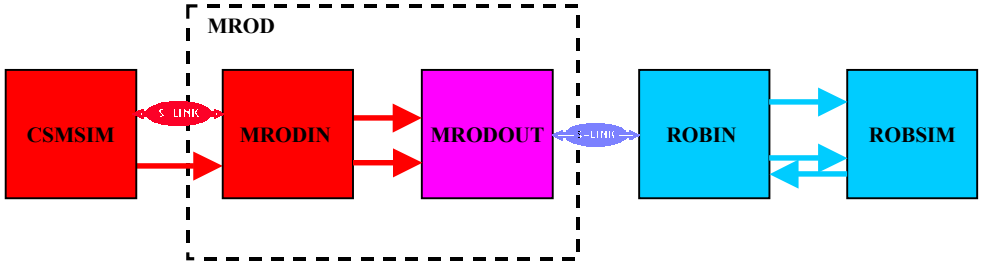

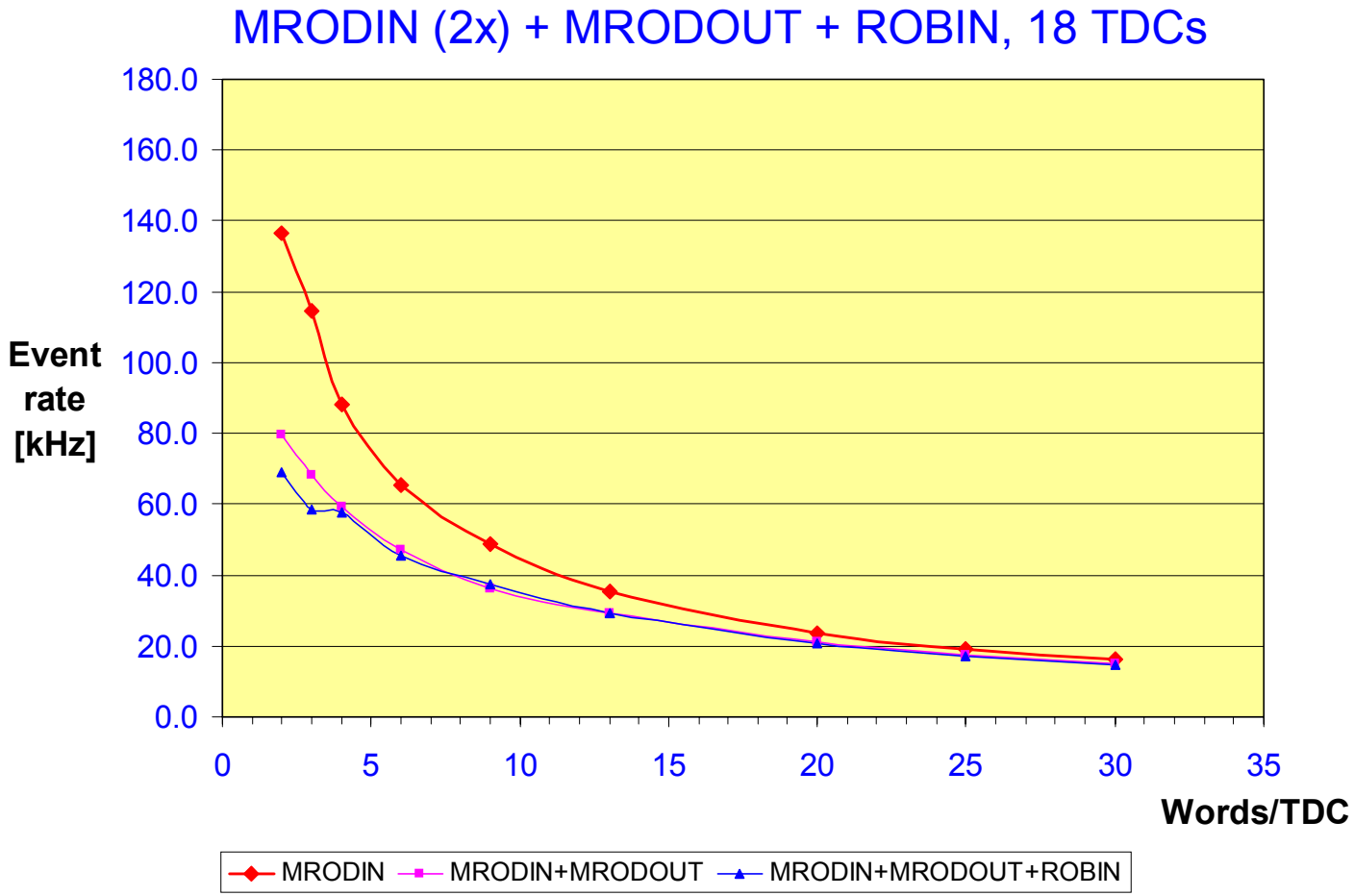

MROD

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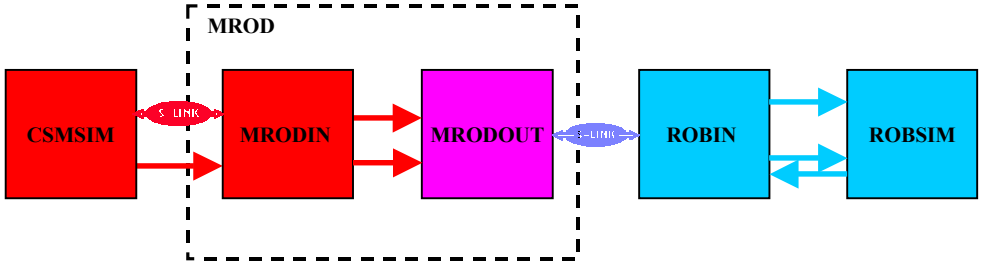

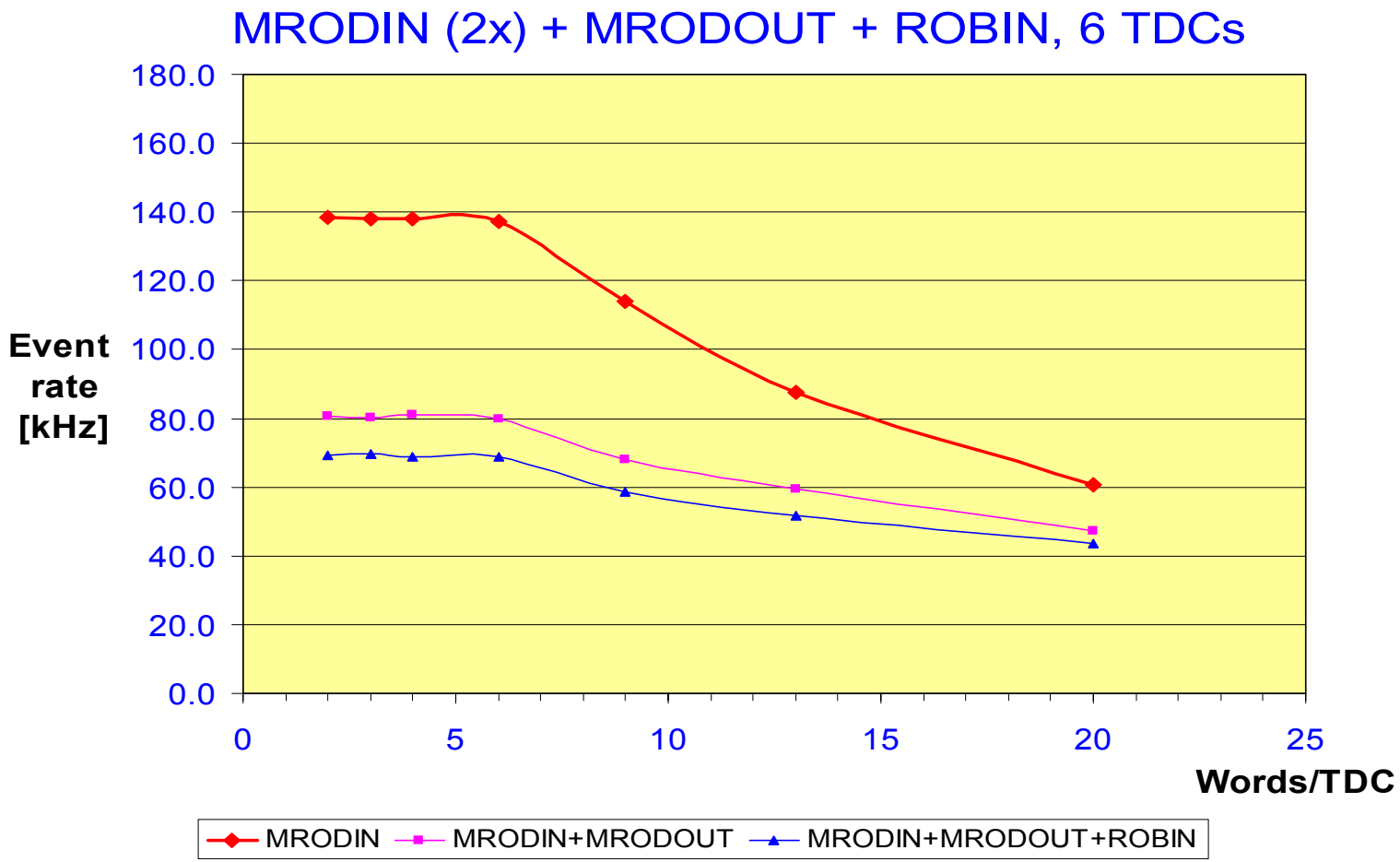

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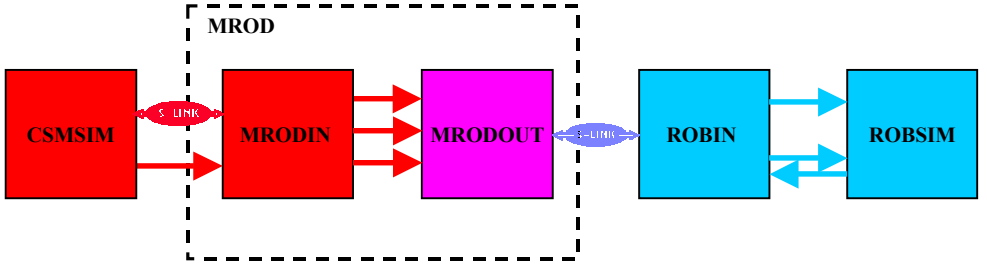
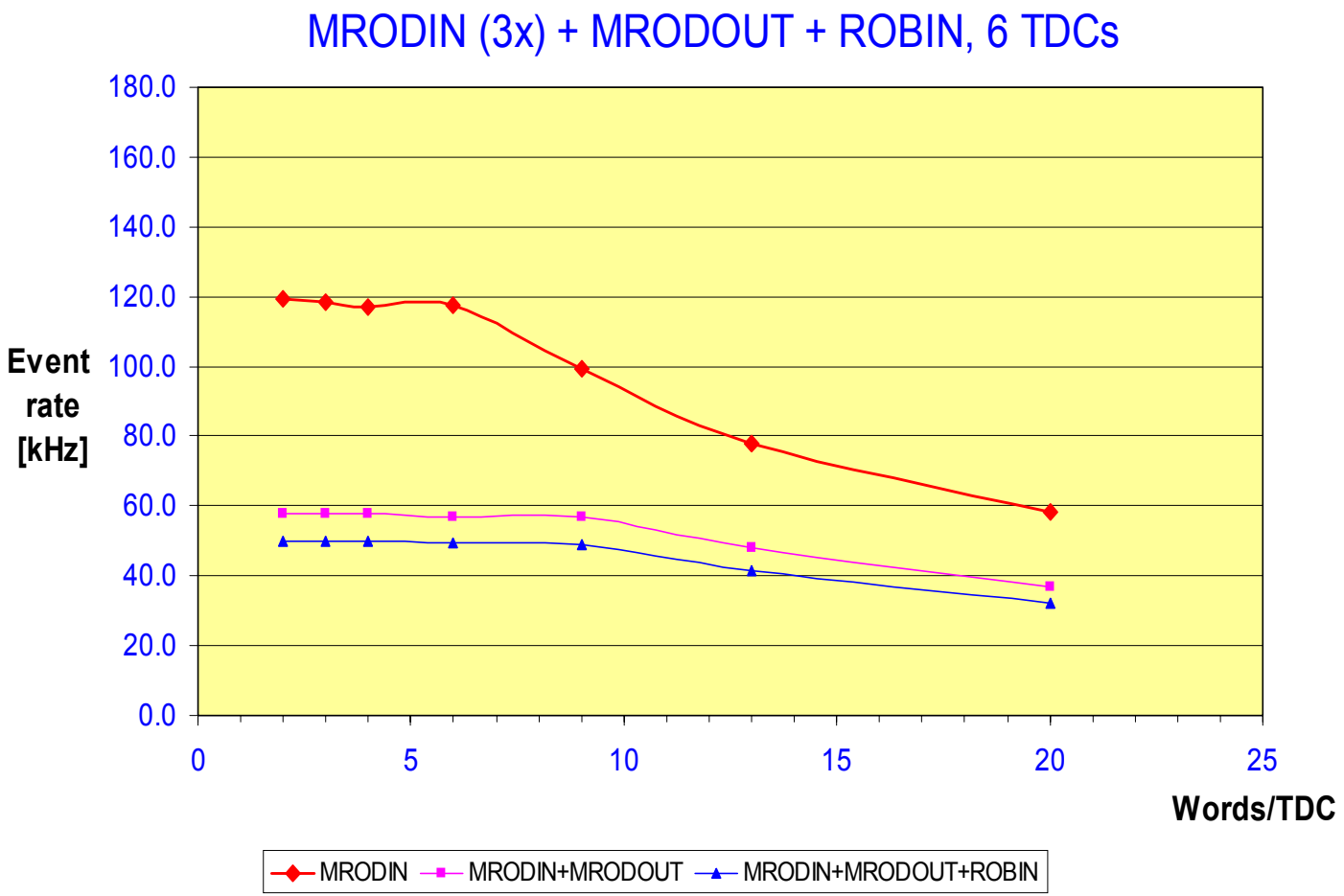
Performance Study Results

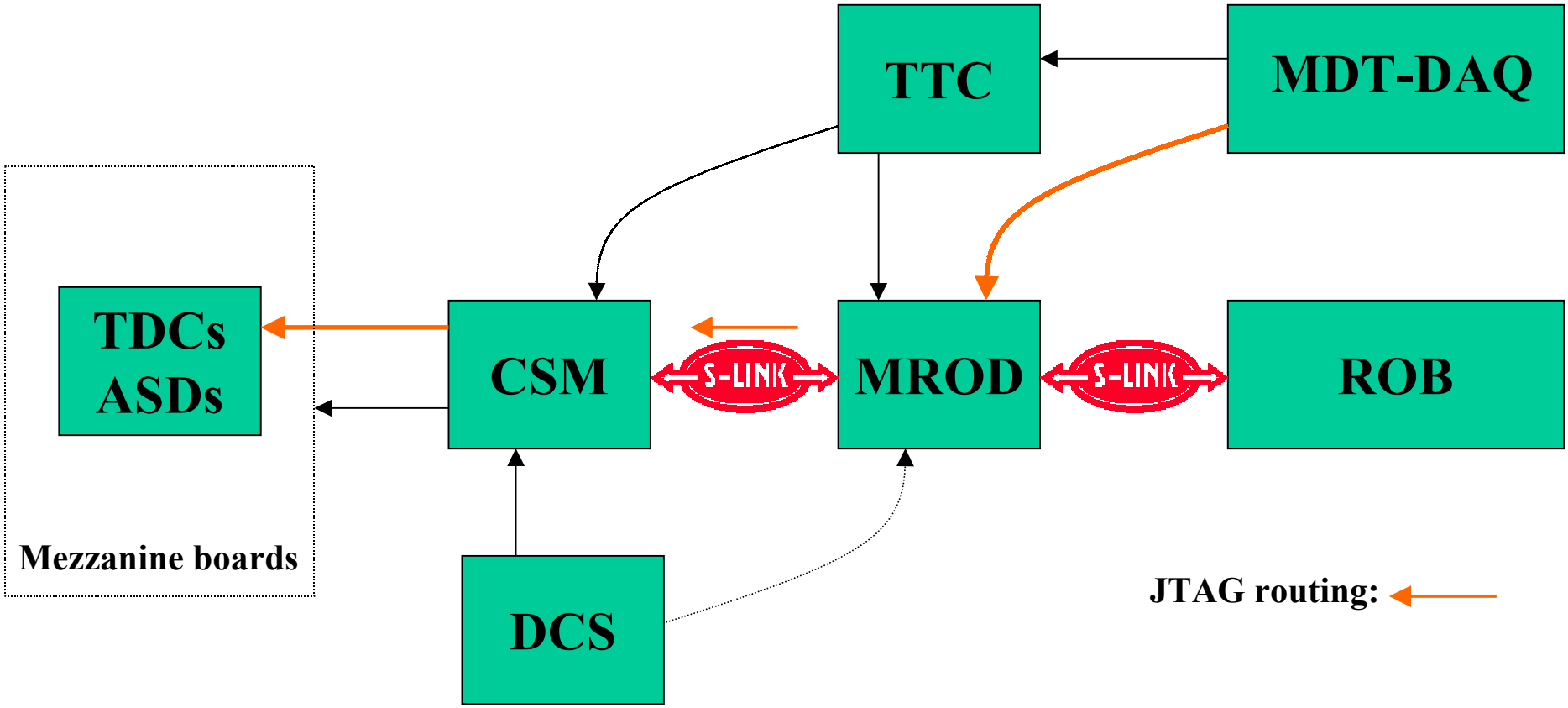




MROD Performance Analysis

- Measured event rate for single output SHARC @ 40 MHz with 3 input channels: event rate ≈ min(50,1000/(10 + #words-per-CSM/6) kHz.
- MROD-1 uses SHARC-II @ 80 MHz: both processing speed and bandwidth increase proportionately → event rate ≈ 100 kHz ?
- 'Final' MROD: SHARC-II @ ≥100 MHz.

FE parameter loading/initialization



JTAG Usage

- Initialize/Set/Reset ASD/TDC/CSM parameters
- Reload CSM Flash Memory (if/when needed)
- Calibration sequence:

  1: JTAG enables calibration pulses in the ASD

  2: TTC signals the CSM to send a test pulse

  3: TTC provides calibration trigger

$\rightarrow$ No calibration during regular data taking.

MROD Names (NIKHEF and Univ.of Nijmegen)

- Henk Boterenbrood
- Peter Jansweijer
- Gerard Kieft
- Adriaan König
- Jos Vermeulen
- Thei Wijnen
- NN (Post-doc vacancy at Univ.of Nijmegen: www.hef.kun.nl/vac-postdoc.html)